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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,479	09/09/2003	Jung-Suk Goo	039153-0676 2044	
23392 7	7590 08/25/2004		EXAM	INER
FOLEY & LARDNER			TRINH, HOA B	
2029 CENTURY PARK EAST SUITE 3500			ART UNIT	PAPER NUMBER
LOS ANGELES, CA 90067			2814	-

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

(	Application No.	Applicant(s)				
Office Action Comment	10/658,479	GOO ET AL.				
Office Action Summary	Examiner	Art Unit				
	Vikki H Trinh	2814				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	86(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. O (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on						
2a) ☐ This action is <b>FINAL</b> . 2b) ☒ This	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
3) Since this application is in condition for allowar	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-20</u> is/are pending in the application.	4)⊠ Claim(s) <u>1-20</u> is/are pending in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-6 and 8-20</u> is/are rejected.						
· <u> </u>	7)⊠ Claim(s) <u>7</u> is/are objected to.					
8) Claim(s) are subject to restriction and/or	r election requirement.					
Application Papers						
9) ☐ The specification is objected to by the Examine						
10)⊠ The drawing(s) filed on <u>09 September 2002</u> is/are: a)⊠ accepted or b) $\square$ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correcting 11) The oath or declaration is objected to by the Ex						
Priority under 35 U.S.C. § 119						
12) ☐ Acknowledgment is made of a claim for foreign a) ☐ All b) ☐ Some * c) ☐ None of:	priority under 35 U.S.C. § 119(a)	-(d) or (f).				
1. Certified copies of the priority documents have been received.						
<ul> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage</li> </ul>						
·	•	ed in this National Stage				
application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
God the uttashed detailed Ginoc detail for a list	of the definied depice not receive	<b>u</b> .				
Attachment(s)						
1) Notice of References Cited (PTO-892)	4) Interview Summary Paper No(s)/Mail Da					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) Notice of Informal P	atent Application (PTO-152)				
Paper No(s)/Mail Date 6) Li Other:						

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#### **DETAILED ACTION**

### Claim Objections

1. Claim 9 is objected to because of the following informalities: in lines 5-6, "a gate insulator" should be "the gate insulator". Appropriate correction is required.

## Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  - 1. Determining the scope and contents of the prior art.
  - 2. Ascertaining the differences between the prior art and the claims at issue.
  - 3. Resolving the level of ordinary skill in the pertinent art.
  - 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
- 3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 4-6, 8-14 and 16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), figures 1-2, in view of Fossum (6,744,084)

APA discloses a method for forming a metal oxide semiconductor field effect transistor (MOSFET), comprising the steps of providing a substrate 10 (fig. 1) comprising a layer of silicon germanium 32 (fig. 2) grown on an underlying silicon layer 10 (fig. 2); forming trenches 12 in the silicon germanium 32 layer to define an active region 16 of the MOSFET; forming isolations 12 in the trenches, the isolations comprising; and forming a MOSFET 17 on the substrate in the active region, the MOSFET comprising a layer of strained silicon 34 (fig. 2) formed on the silicon germanium 32 in the active region 16 (fig. 2).

However, APA does not explicitly teach that the isolations 12 included a high thermal conductivity insulating material made of silicon carbide.

Fossum (6,744,084) teaches a semiconductor device having isolations 150 (fig. 7) that are filled with a high thermal conductivity insulating material, silicon carbide (col. 4, line 7), and a thin oxide liner formed on the sidewalls and bottom of the trench (col. 4, lines 25-29).

Therefore, as to claims 1, 4 and 6, it would have been obvious to one skilled in the art at the time the invention was made to modify the isolation in the trench of APA with an oxide liner and the high thermal insulating material, silicon carbide, as taught by Fossum, so as to provide adequate pathway for heat dissipation in the device.

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As to claim 5, the combined teaching of APA in view of Fossum would also result in the same effect as claimed, whereby the high thermal conductivity insulating material has a thermal conductivity higher than the thermal conductivity of silicon.

As to claim 8, APA teaches a strained silicon layer 34 (fig. 2) is formed on the silicon germanium prior to forming the trenches, and wherein the trenches are formed in the strained silicon layer (fig. 2) and the silicon germanium layer 32 (fig. 2).

As to claim 9, APA teaches the steps of forming a gate insulating layer 18 (fig. 2) on the strained silicon layer 34; forming a gate conductive layer 14 on the gate insulating layer 18; and patterning the gate conductive layer to form a gate 14 overlying the gate insulator 18 (fig. 2)

As to claim 10, APA teaches the steps of forming a first spacer 30 (fig. 1, or fig. 2)) around the gate 14; and implanting shallow source and drain extensions 28 (fig. 1, or fig. 2).

As to claim 11, APA teaches the steps of forming a second spacer 22 (fig. 1, or fig. 2); implanting deep source 24 and drain regions 24 (fig. 1, fig. 2) wherein the second spacer serves as an implantation mask during implanting the deep source and drain regions 24 (fig. 2).

As to claim 12, APA teaches the step of forming nickel silicide source and drain contacts (spec., page 1, line 29) and a nickel silicide gate contact (spec., page 1, line 29).

As to claim 13, APA teaches that the composition for silicon germanium is within the range (spec., page 4, lines 2-4) as claimed.

As to claims 14, 16, 18 and 20, APA discloses a substrate with a silicon germanium 32 on a silicon layer 10 and a strained silicon channel region 16 (fig. 2); a gate 14 overlying the channel region and separated from the channel by a gate insulator 18 (fig. 2); source and drain regions

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20(fig. 2) formed in the silicon germanium; and shallow trench isolations 12 (fig. 2) formed in the silicon germanium layer 232 and defining an active region 16 of the MOSFET (fig. 2).

However, APA does not explicitly teach that the isolations 12 included a high thermal conductivity insulating material made of silicon carbide.

Fossum (6,744,084) teaches a semiconductor device having isolations 150 (fig. 7) that are filled with a high thermal conductivity insulating material, silicon carbide (col. 4, line 7), and a thin oxide liner formed on the sidewalls and bottom of the trench (col. 4, lines 25-29).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the isolation in the trench of APA with an oxide liner and the high thermal insulating material, silicon carbide, as taught by Fossum, so as to provide a good material against heat built-up in the device.

As to claim 19, the combined teaching of APA in view of Fossum would also result in the same effect as claimed, whereby the high thermal conductivity insulating material has a thermal conductivity higher than the thermal conductivity of silicon.

5. Claims 2-3, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), figures 1-2, in view of Fossum (6,744,084), and further in view of Eshita (4,994,413)

The combined teaching of APA in view of Fossum describes the invention substantially as claimed. However, the combined teaching of both references does not disclose that the trench formed in the silicon germanium layer exposes the underlying silicon layer and that the isolations contact the silicon layer, or that the high thermal conductivity insulating material of the isolations contacts the silicon layer.

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Eshita teaches a semiconductor device having a substrate with a silicon layer 51 and two SiC layers 53 and 52 (fig. 5E). Eshita also teaches that a trench with an isolation 55 extending from the SiC layers to the silicon layer 51, thereby exposing the silicon layer 51 (fig. 5E). The isolation material contacts the silicon layer 51. (fig. 5E).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the combined teaching of APA in view of Fossum with the isolation being extended to the silicon layer and thereby exposing and in contact with the silicon layer, as taught by Eshita, so as to provide an enhance the drive current in the device.

## Allowable Subject Matter

- 6. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 7. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach either in singly or in combination a method of forming MOSFET having the steps of forming a layer of silicon carbide over the substrate to fill the trenches and planarizing the silicon carbide to form the isolations in the trenches, and other steps in the claims.

#### Conclusion

1. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the

Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <a href="http://pair-direct.uspro.gov">http://pair-direct.uspro.gov</a>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <a href="http://www.uspto.gov/ebc/index.html">http://www.uspto.gov/ebc/index.html</a> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh, Patent Examiner AU 2814

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